2.8 GBIT/S OPTICAL INTERCONNECTION CIRCUIT USING D8B1C/D8B1M CODING SCHEME

Y. Uematsu, K. Murata, Y. Yamabayashi and Y. Kobayashi

NTT Optical Network Systems Laboratories
Kanagawa, Japan

Abstract

We develop a 2.8 Gbit/s optical interconnection circuit using the D8B1C (Differential 8 Binary 1 Complement insertion) /D8B1M (Differential 8 Binary with 1 Mark insertion) coding scheme for multiplexed channel framing and synchronization and suppressing Direct Current level variation. The circuit multiplexes 16 parallel 156 Mbit/s input signals, and outputs a 2.8 Gbit/s serial signal. The coding scheme, named D8B1C/D8B1M, realizes large capacity interconnections with simple analog circuits, and offers high flexibility for extension to higher capacity interconnections.

Introduction

For Broadband ISDN and multi-media services, transmission system capacities of tens or hundreds of giga-bits per seconds are needed. Very high transmission bit rates demand large capacity shelf-to-shelf and/or package-to-package interconnections. For these demands, various kinds of parallel optical data links which have several giga-bits per second throughputs have been reported. [1][2] However, these parallel interconnections depend on highly reliable laser diodes arrays, low coupling loss variation between laser and fiber, and the accurate compensation of phase skew among data channels. Multiplexed serial transmissions seem more feasible because they avoiding these difficulties.

In order to realize high-speed multiplexed serial data links, there are two points to be solved. First is multiplexed channel framing and synchronization. The second is suppressing Direct Current level variation. Several kinds of coding scheme for these requirements have been reported such as the mB1C code [3] and DmB1M code [4]. However, these coding schemes are not suitable because of the complexity of the decoder.

This paper describes a new coding scheme called the DmB1C (Differential m Binary 1 Complement insertion) /DmB1M (Differential 8 Binary with 1 Mark insertion) code which can realize multiplexed channel framing and synchronization with simple circuit construction. The coding format has several benefits such as low line rate increase, short maximum consecutive length and good balance in the number of 0s and 1s of the signals. We apply the D8B1C/D8B1M coding scheme to a 2.8 Gbit/s optical multiplexed serial intra system with sixteen 156 Mbit/s parallel inputs and experimental results are shown.

DmB1C/DmB1M Code

Figure 1 shows the block diagrams of the DmB1C/DmB1M encoder and decoder. The signal processing sequence for the case of m=8 is shown in figure 2. In DmB1C coding, the speed of the input signal (PC) is increased by (m+1)/m, and the complementary bit of the m th time slot is inserted into the (m+1) th time slot. The mB1C code (QC) is converted into the DmB1C code (SC) by the following equation using a finite sum operation circuit.

$$SC_k = SC_{k-1} \oplus QC_k \qquad (1)$$

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where SCk and QCk denote the k th signal bit of SC and QC, respectively. The symbol $\oplus$ denotes logical exclusive OR. Considering the relationship between the (m+1) th and m th bit of SC in (1), the following equation can be derived;

$$SCm+1 = SCm-1 \oplus QCm \oplus QCm+1.$$

As QCm+1 is always the complement of QCm,

$$SCm+1 = SCm-1 \oplus 1$$
$$SCm+1 = \overline{SCm-1} \quad (2)$$

where, $\overline{SCm-1}$ denotes the complement of SCm-1. This means that SCm+1 is always the complement of SCm-1, and the maximum number of consecutive identical digits is m+2 bits in the DmB1C code.

In DmB1M coding, the speed of the input signal (PM) is increased by (m+1)/m, and a mark bit is inserted into the (m+1) th time slot. the mB1M code (QM) is converted into DmB1M code (SM) by equation (1) using the same circuit used for DmB1C coding. Considering the m+1 th bit of SM in (1) and QMm+1 are always mark bits

$$SMm+1 = SMm \oplus 1$$
$$SMm+1 = \overline{SMm} \quad (3)$$

where, $\overline{SMm}$ denotes the complement of SMm. This means that SMm+1 is always the complement of SMm, and the maximum number of consecutive identical digits is m+1 bits in the DmB1M code. The number of 0s and 1s in the signals for the D8B1C code and the D8B1M code is always equal for input signals of any mark ratio. [4]

When decoding DmB1C and DmB1M codes, the mB1C code (QC) and mB1M code (QM) are obtained by the following equations using a finite difference operation circuit.

$$QC_k = SC_k \oplus SC_{k-1} \quad (4\text{-}1)$$

$$QM_k = SM_k \oplus SM_{k-1} \quad (4\text{-}2)$$

The original information signals PC and PM are then recovered through m/(m+1) speed conversion.

DmB1C/DmB1M coding is realized by combining the bit multiplexing of a DmB1C code (SC) and a DmB1M code (SM). On the other hand, DmB1C/DmB1M decoding is realized by demultiplexing the input signals as shown in Fig. 1. The DmB1C/DmB1M coding scheme easily supports increased numbers of channels because the mB1C and mB1M decoding circuits can be used in common. In order to increase transmission capacity, we need only to exchange the bit multiplexer and demultiplexer. The code characteristics of DmB1C, DmB1M and DmB1C/DmB1M are summarized in table 1.

Circuit Configuration

To verify the DmB1C/DmB1M coding scheme, we developed a proof-of-concept intra system that transmits sixteen 156 Mbit/s signals. Its circuit diagram is shown in figure 3. In this system, the 156 MHz system clock is provided to the transmitter and receiver.

The transmitter consists of the D8B1C/D8B1M coding circuits shown in Fig.1(a), an E/O converter and a 2.8 GHz clock generator. An 8B1C and an 8B1M encoder were constructed using two 9:1 multiplexers, so D8B1C/D8B1M encoder is very simple. The E/O converter consists of a Fabry-Perot laser diode and its driver IC. The 2.8 GHz clock signal was generated from the 156 MHz clock signal by an 18 times frequency up-converter, which consists of a double feed back loop type PLL.

The receiver consists of an O/E converter, the D8B1C/D8B1M decoding circuit shown in Fig.1(b) and a 2.8 GHz clock generator. The O/E converter consists of a PIN-PD and a limiting amplifier and decision circuit. 8B1C and 8B1M coded signals are decoded by two 1:9 demultiplexers, 8B1C and 8B1M decoder circuits. An 8B1C and an 8B1M decoder are fabricated on the same 1.7 K-gate Si bipolar LSI. The LSI has the functions of automatic output channel selection and coding scheme type detection. [5]

The circuit configuration of the D8B1C/D8B1M encoder and decoder is very simple.

Experimental Results

The interconnection circuit was tested and evaluated by connecting a transmitter and a receiver with a 1.3 μm zero dispersion fiber. Sixteen 156 Mbit/s input signals with PN 7 pseudo random signals were used and the error rate of each channel output by the receiver was measured. Error free operation was successfully confirmed. Figure 4 shows D8B1M coding signal of the transmitter, D8B1C/D8B1M coding signal at the DEC output of the receiver module, and D8B1C and D8B1M decoding signal at the finite difference circuit output of the receiver. The 2.8 GHz clock generator operated stably. The output spectrum of 2.8 GHz clock signal is shown in figure 5.

The interconnection circuit was mounted on a package consisting of a mother board and a daughter board. The 2.8 GHz clock generator was mounted on the daughter board and the other circuits were mounted on the mother board. The realized package size was 194 mm x 280 mm x 55 mm. A photograph of the board is shown in figure 6.

Conclusion

We have successfully developed a 2.8 Gbit/s optical interconnection circuit using the D8B1C/D8B1M coding scheme. Interconnections based on the DmB1C/DmB1M coding scheme offer large capacity with simple analog circuits, and have high flexibility for extension to higher capacities.

Acknowledgment

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References

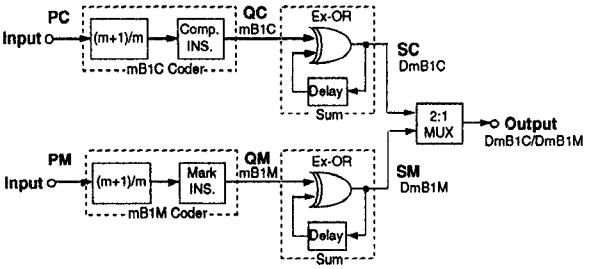
[1] N.Fujimoto, et al. "Line-coding process based on multiplexing for parallel optical transmission", OFC'94 Technical Digest WC4, pp.83 - 84, 1994.

[2] Y. Ota, et al. "Multichannel 4-Gbit/s (500-Mbit/s-per-channel) parallel optical data link", OFC'93 Technical Digest ThC2, pp.167 - 168, 1993.

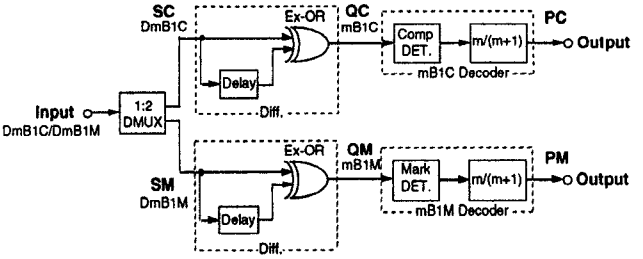
[3] N.Yoshikai, et al. "mB1C Code and Its performance in a Optical Communication System", IEEE Transactions on Communications, Vol. 32, No.2, pp. 163-168. 1984.

[4] S. Kawanishi, et al. "DmB1M Code and its Performance in a Very High-Speed Optical Transmission System", IEEE Transactions on Communications, Vol. 36, No.8, pp. 951-956. 1988.

[5] Y. Yamabayashi, et al. "Line Codings for Optical Transmission (II)", Proc. IEICE Spring Conf. '92, B-789.



(a) DmB1C/DmB1M encoder



(b) DmB1C/DmB1M decoder

Figure 1 Block diagrams of DmB1C/DmB1M encoder and decoder

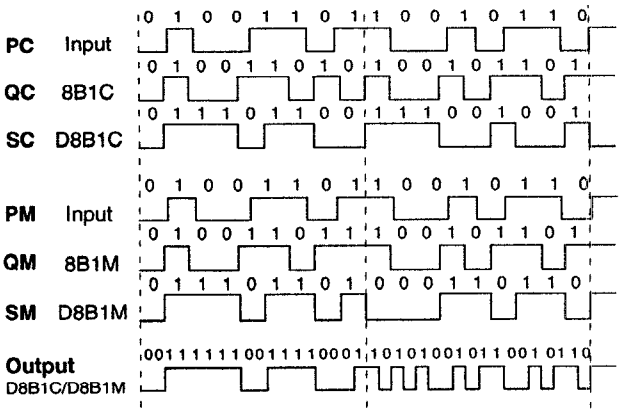


Figure 2 Signal sequences of DmB1C/DmB1M code (m = 8)

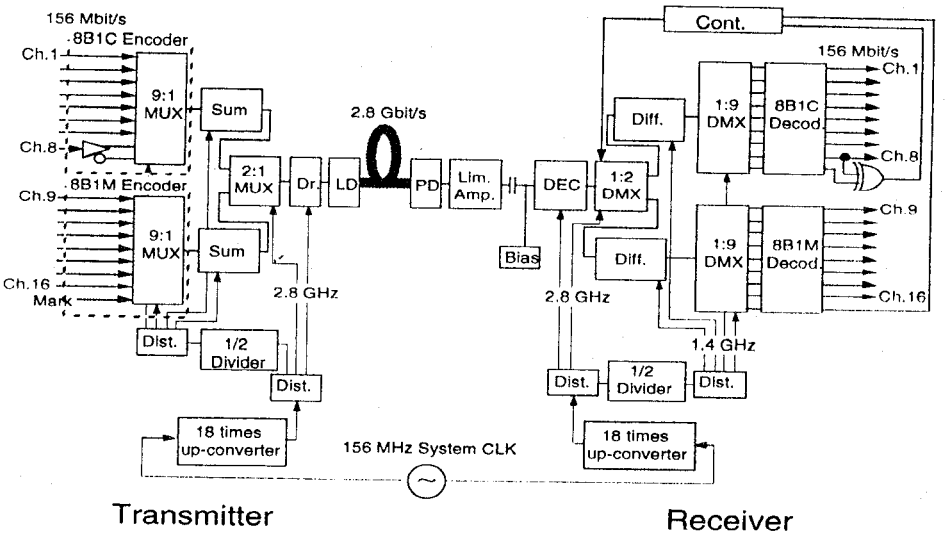
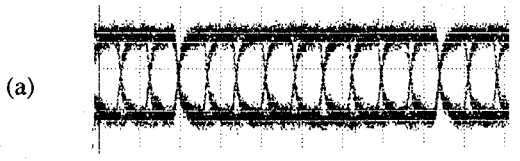
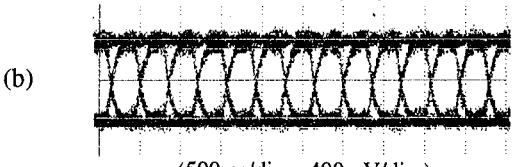


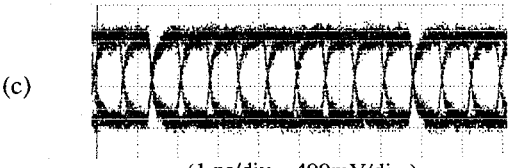
Figure 3 2.8Gbit/s intra system optical interconnection circuit diagram



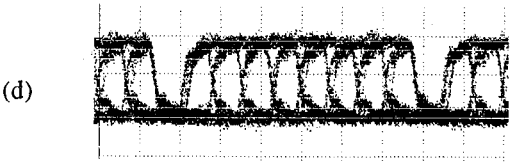
(1 ns/div., 400mV/div.)
(a) D8B1M Encoder Output (1.4 Gbit/s)
----- D8B1M Coding Signal -----



(500 ps/div., 400mV/div.)
(b) DEC Output (2.8 Gbit/s)
----- D8B1C/D8B1M Coding Signal -----



(1 ns/div., 400mV/div.)
(c) D8B1C Decoder Complemental Output (1.4 Gbit/s)
----- 8B1C Coding Signal -----



(1 ns/div., 400mV/div.)
(d) D8B1M Decoder Complemental Output (1.4 Gbit/s)
----- 8B1M Coding Signal -----

Figure 4 Operating waveforms

Table 1
Characteristics of DmB1C/DmB1M Code

	Increase of Code Rate	Max. Length of Consecutive Identical Digits	Balance of Marks and Spaces
DmB1C	(m+1)/m	m+2	1/2
DmB1M	(m+1)/m	m+1	1/2
DmB1C/DmB1M	(m+1)/m	2m+3	1/2

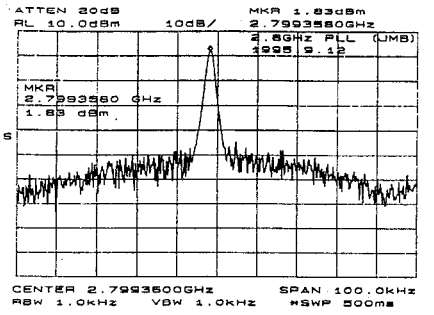


Figure 5 Clock spectrum of 18 times frequency up-conversion

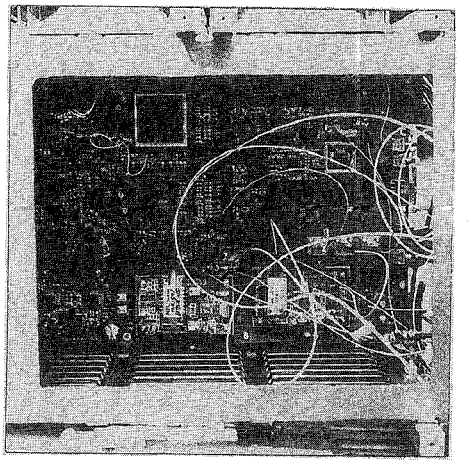


Figure 6 2.8 Gbit/s optical interconnection board